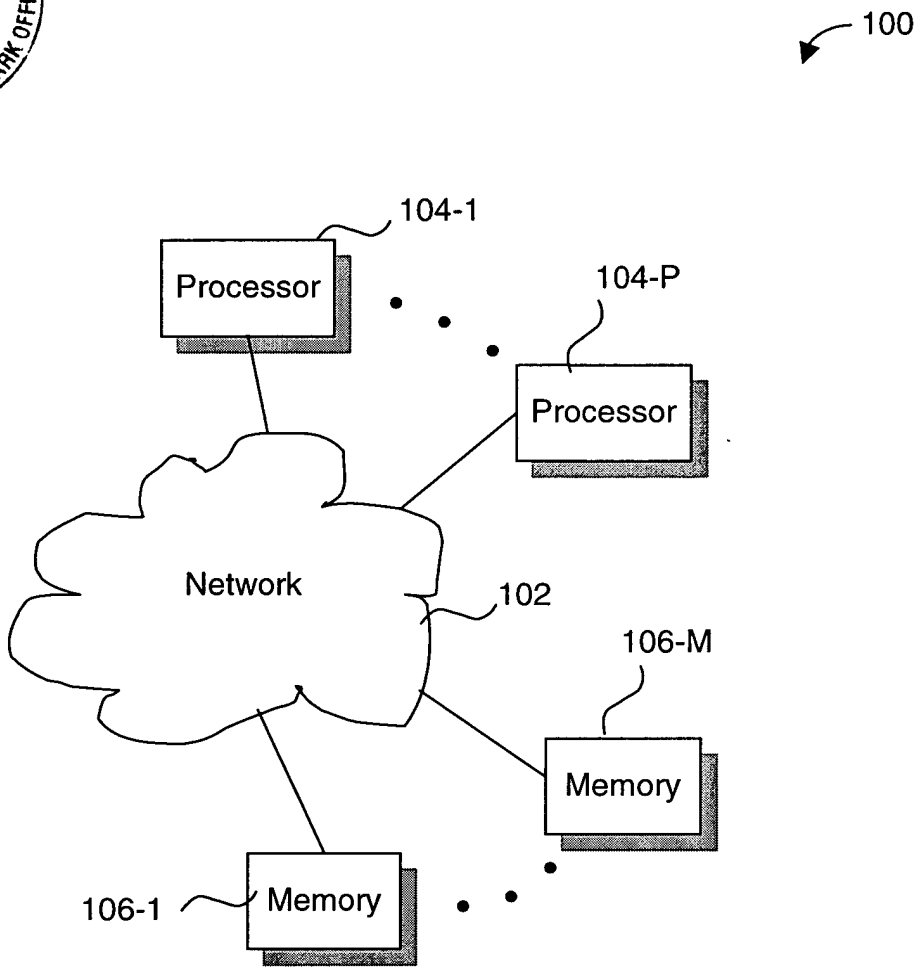

FIG. 1

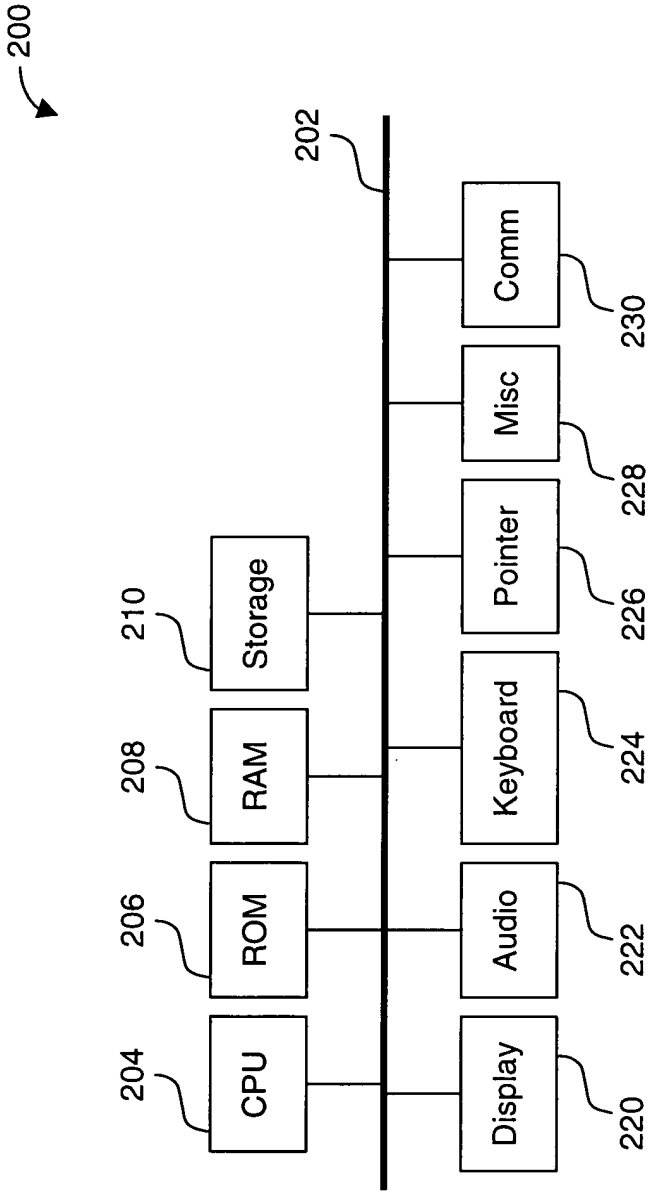
200
202
CPU
204
ROM
206
RAM
208
Storage
210
Display
220
Audio
222
Keyboard
224
Pointer
226
Misc
228
Comm
230

FIG. 2

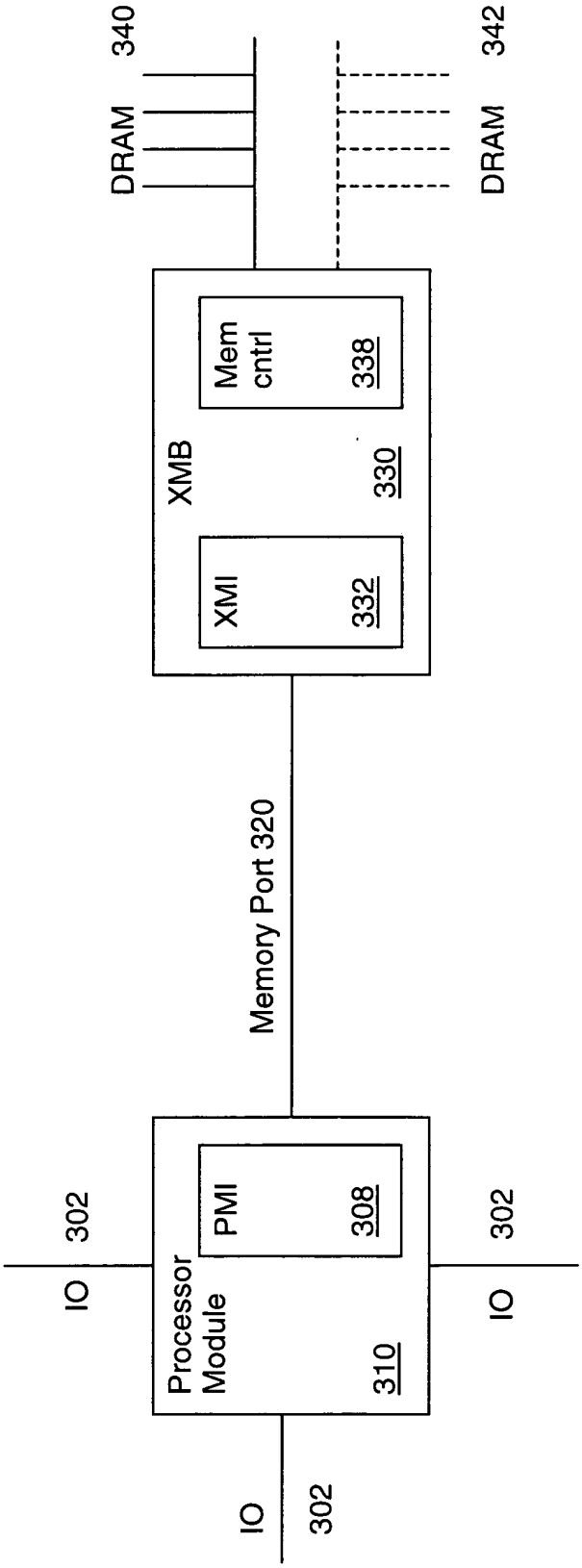
300
DRAM
340
DRAM
342
XMB
Mem cntrl
338
330
XMI
332
Memory Port 320
Processor Module
PMI
308
310
IO
302
IO
302
IO
302

FIG. 3

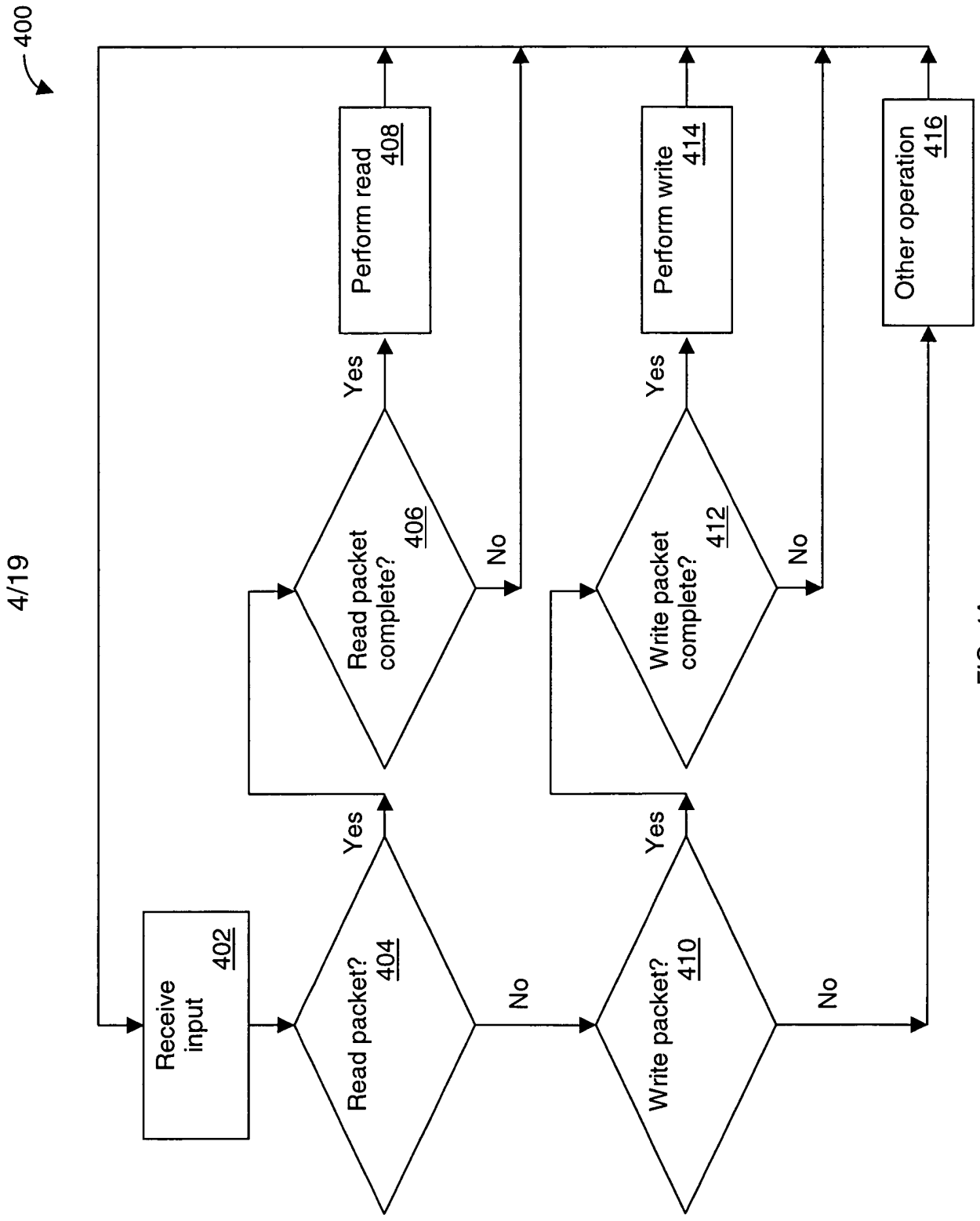
400
Receive input 402
Read packet? 404
Yes
No
Read packet complete? 406
Yes
No
Perform read 408
Write packet? 410
Yes
No
Write packet complete? 412
Yes
No
Perform write 414
Other operation 416

FIG. 4A

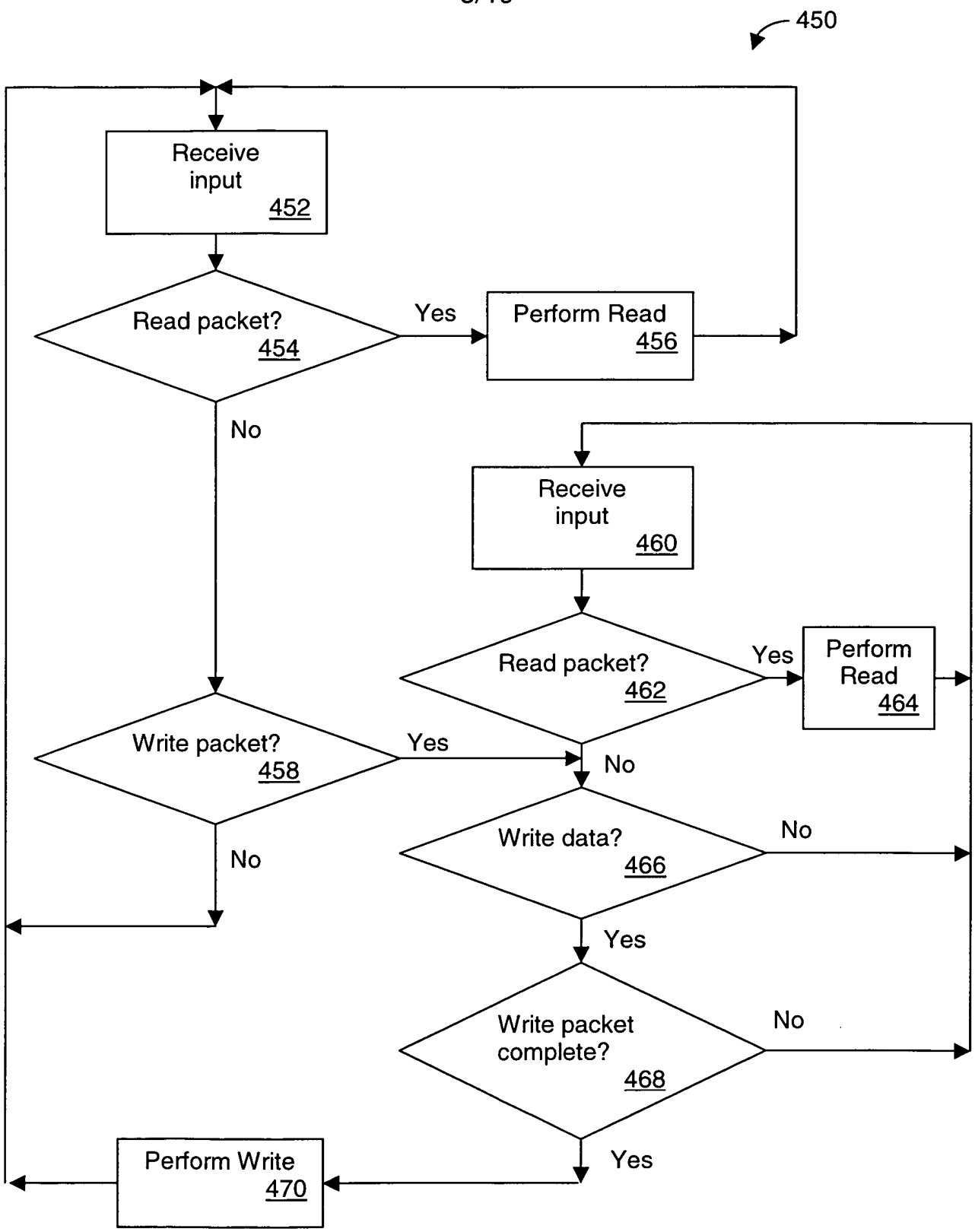
450
Receive input 452
Read packet? 454
Yes
Perform Read 456
No
Receive input 460
Read packet? 462
Yes
Perform Read 464
Write packet? 458
Yes
No
Write data? 466
No
No
Yes
Write packet complete? 468
No
Yes
Perform Write 470

FIG. 4B

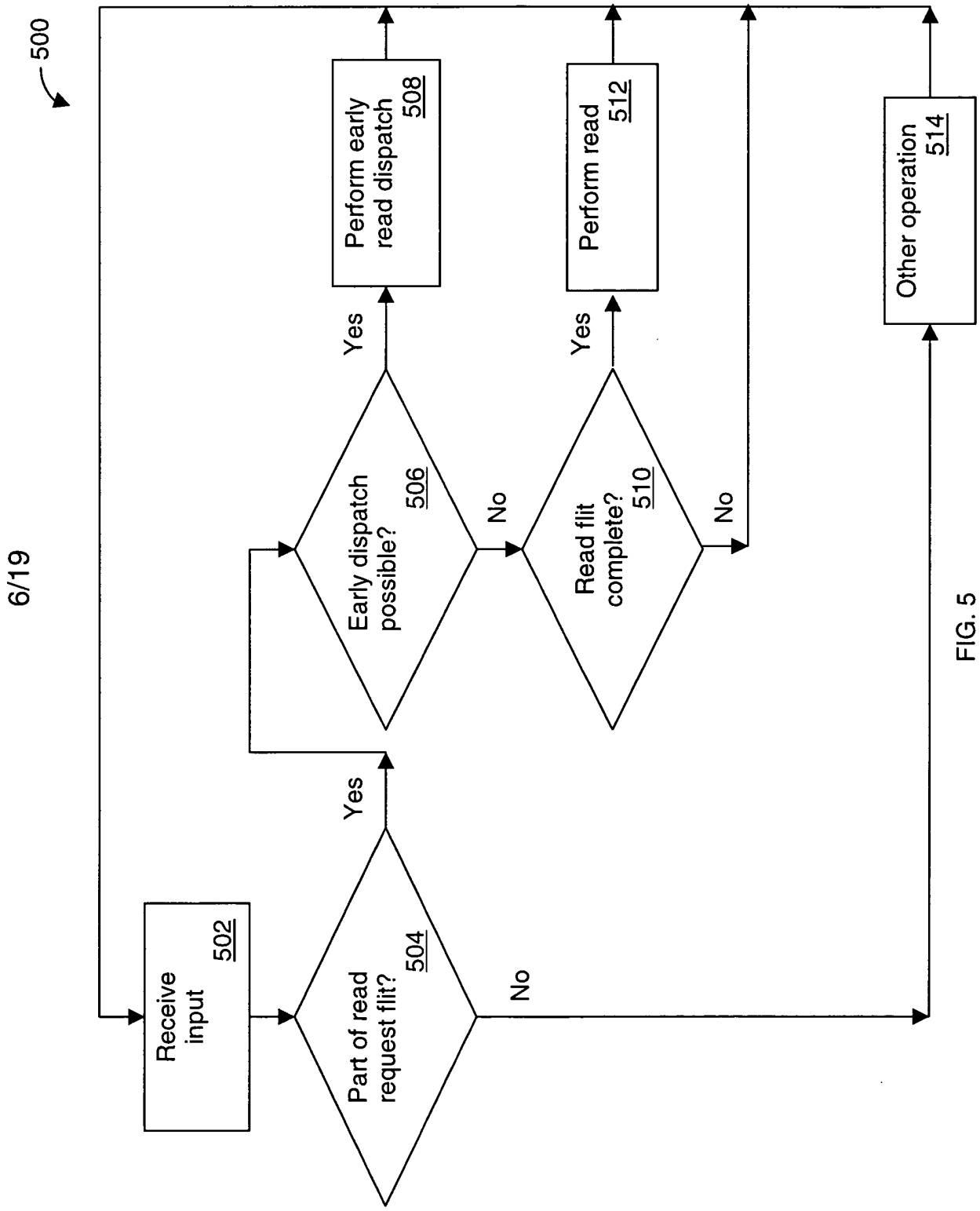
500
Receive input 502
Part of read request flit? 504
Yes
No
Early dispatch possible? 506
Yes
No
Perform early read dispatch 508
Read flit complete? 510
Yes
No
Perform read 512
Other operation 514

FIG. 5

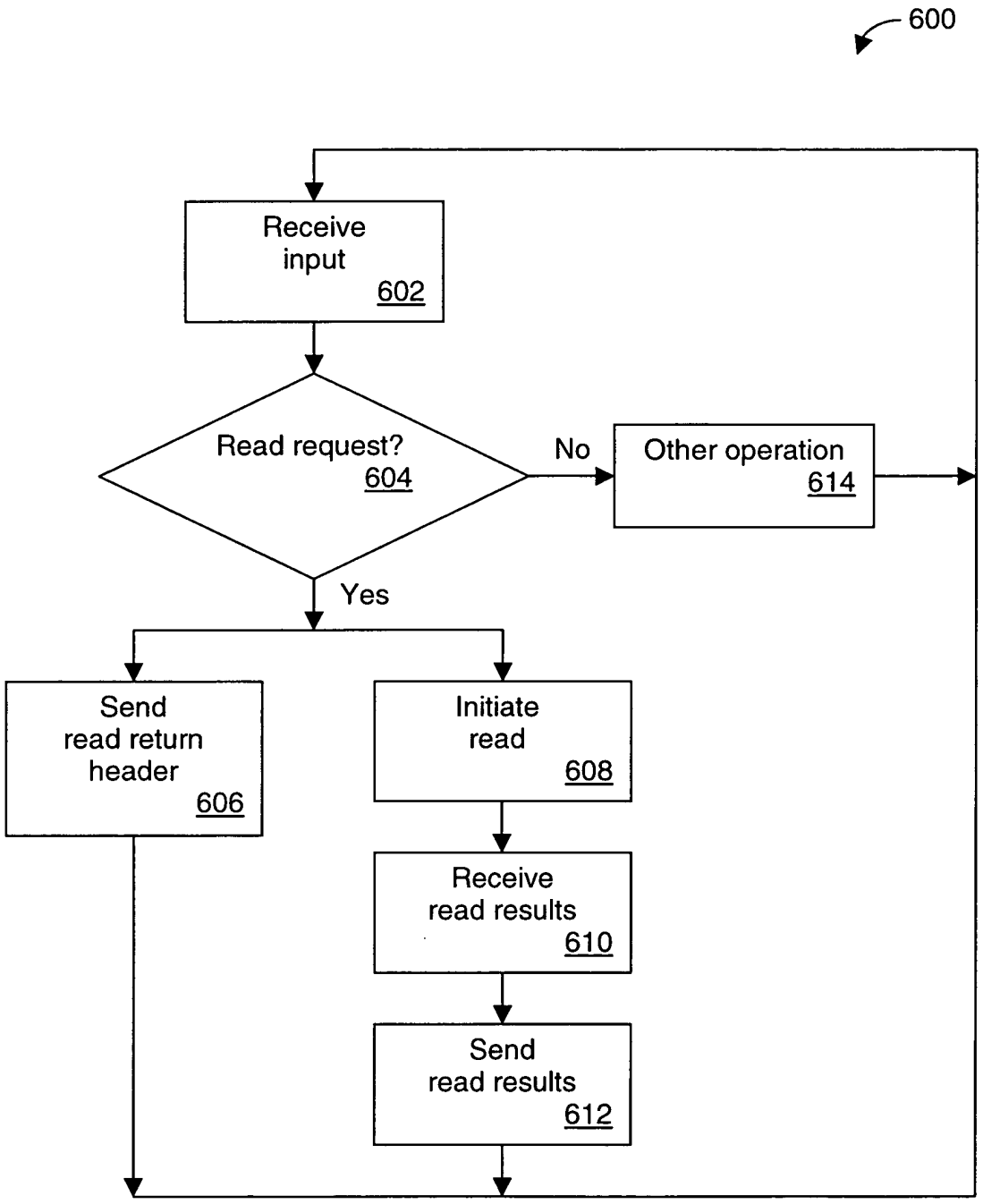
600
Receive input 602
Read request? 604
No
Other operation 614
Yes
Send read return header 606
Initiate read 608
Receive read results 610
Send read results 612

FIG. 6A

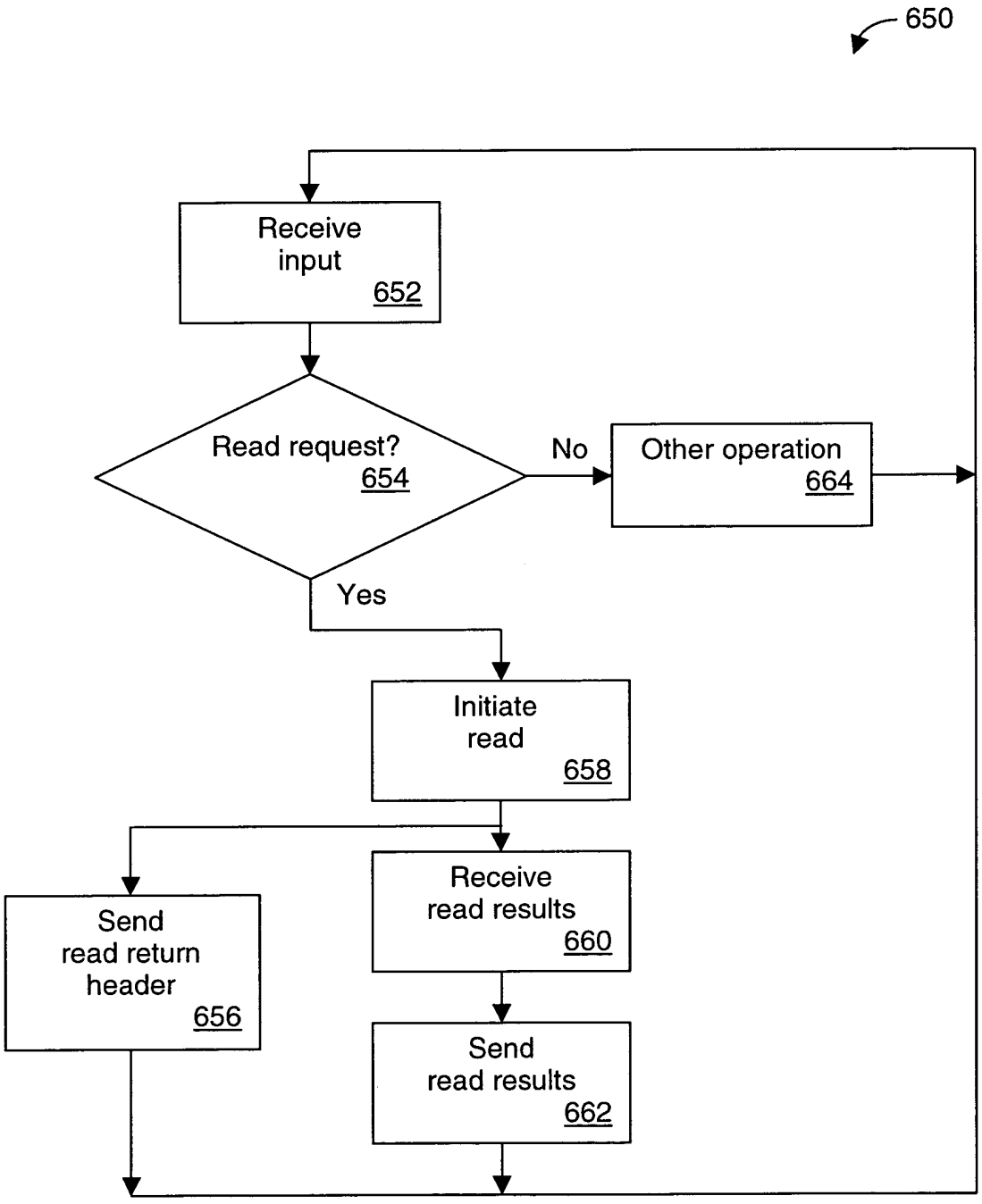
650
Receive input 652
Read request? 654
No
Other operation 664
Yes
Initiate read 658
Send read return header 656
Receive read results 660
Send read results 662

FIG. 6B

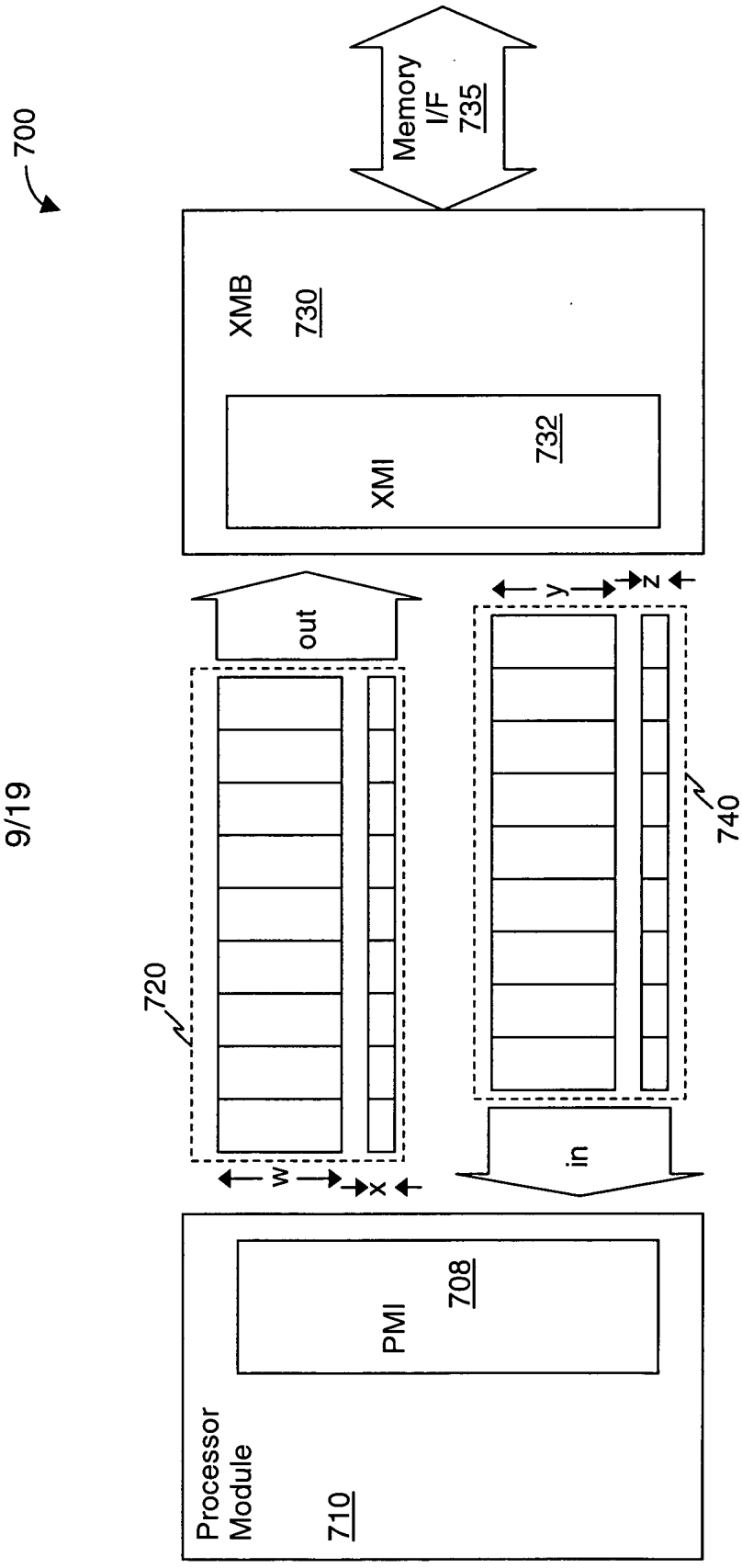
700
Memory I/F 735
XMB 730
XMI 732
out
y
z
720
740
w
x
in
PMI 708
Processor Module 710

FIG. 7

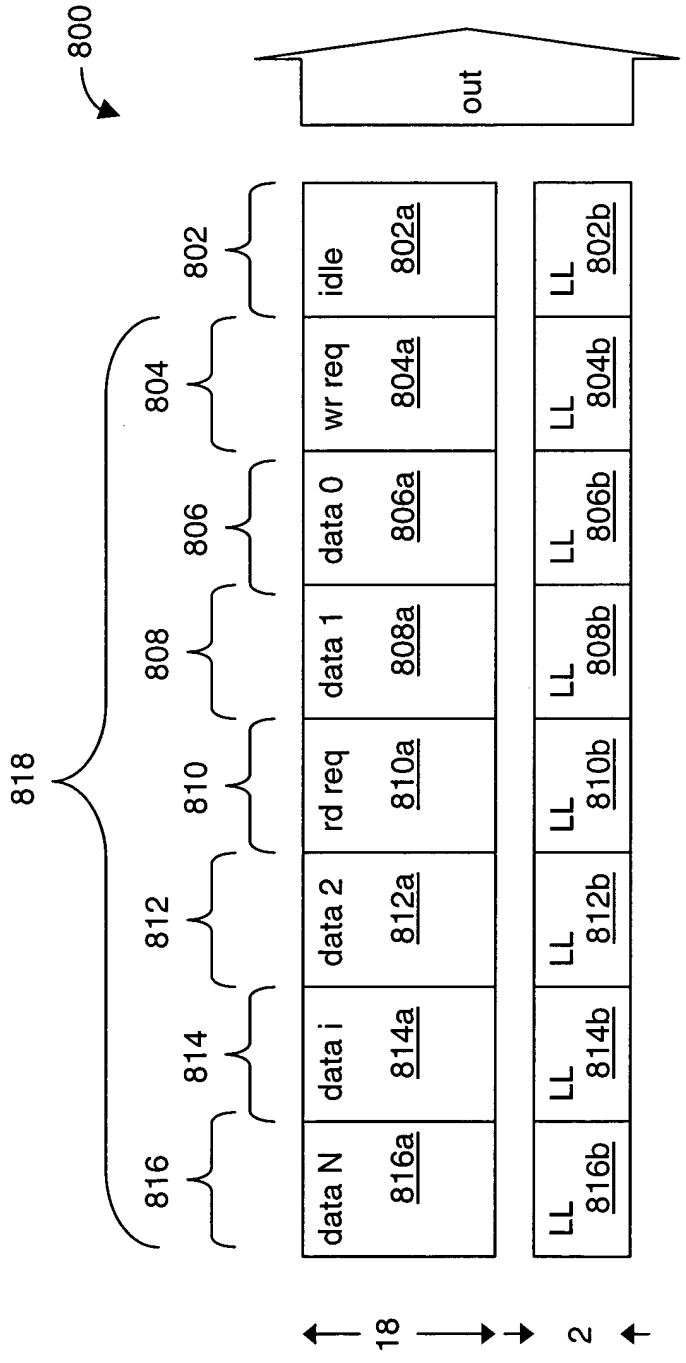
800
out
802
804
806
808
810
812
814
816
818
idle
802a
wr req
804a
data 0
806a
data 1
808a
rd req
810a
data 2
812a
data i
814a
data N
816a
LL
802b
LL
804b
LL
806b
LL
808b
LL
810b
LL
812b
LL
814b
LL
816b
18
2

FIG. 8

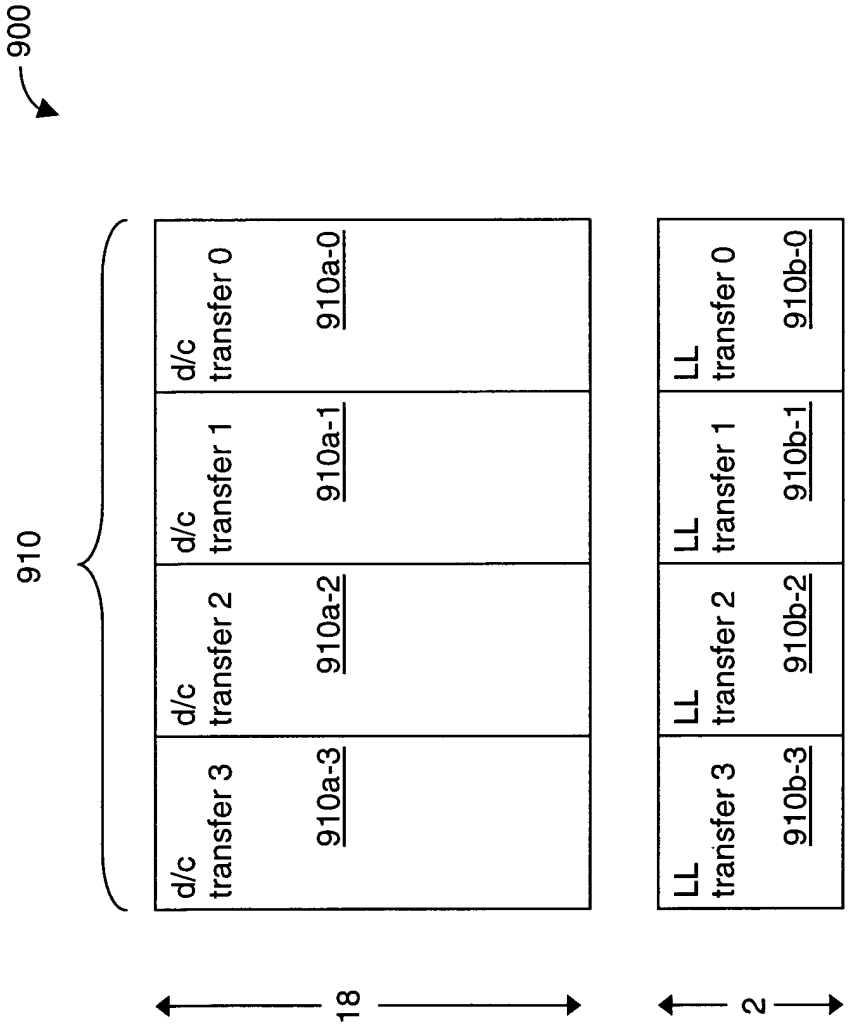
900
910
d/c transfer 3
910a-3
d/c transfer 2
910a-2
d/c transfer 1
910a-1
d/c transfer 0
910a-0
18
LL transfer 3
910b-3
LL transfer 2
910b-2
LL transfer 1
910b-1
LL transfer 0
910b-0
2

FIG. 9

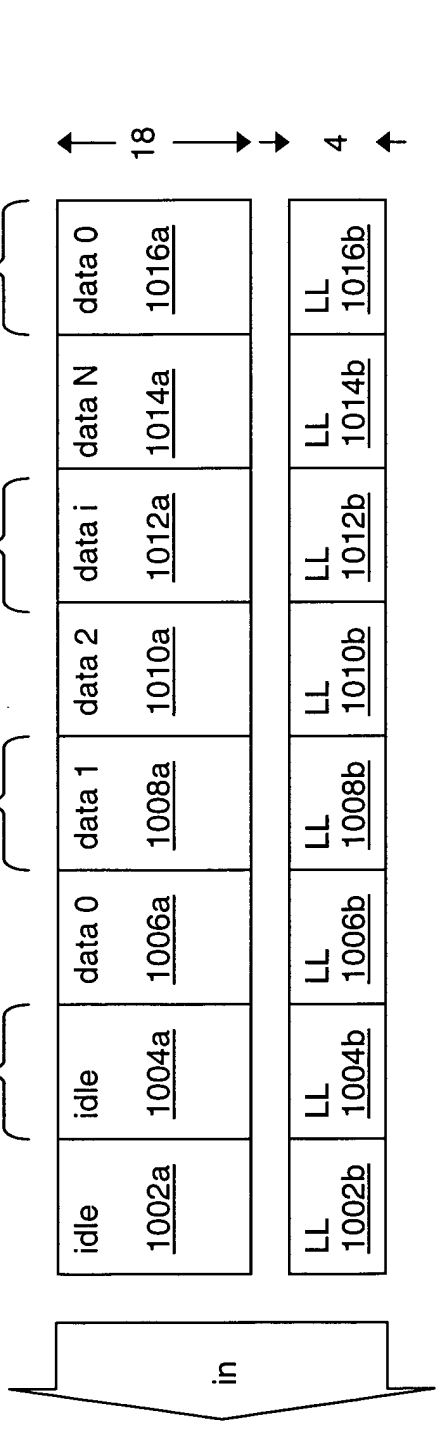
1000
18
4
1002
1004
1006
1008
1010
1012
1014
1016
idle 1002a
idle 1004a
data 0 1006a
data 1 1008a
data 2 1010a
data i 1012a
data N 1014a
data 0 1016a
LL 1002b
LL 1004b
LL 1006b
LL 1008b
LL 1010b
LL 1012b
LL 1014b
LL 1016b
in

FIG. 10

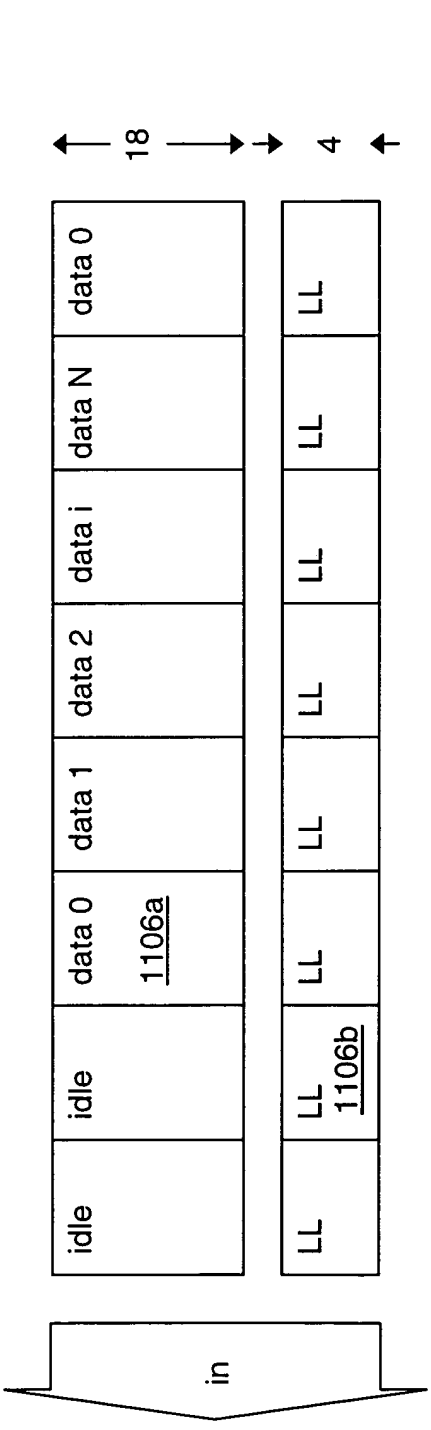
1100
18
4
data 0
data N
data i
data 2
data 1
data 0
idle
idle
LL
LL
LL
LL
LL
LL
LL
LL
1106
1106a
1106b
in

FIG. 11

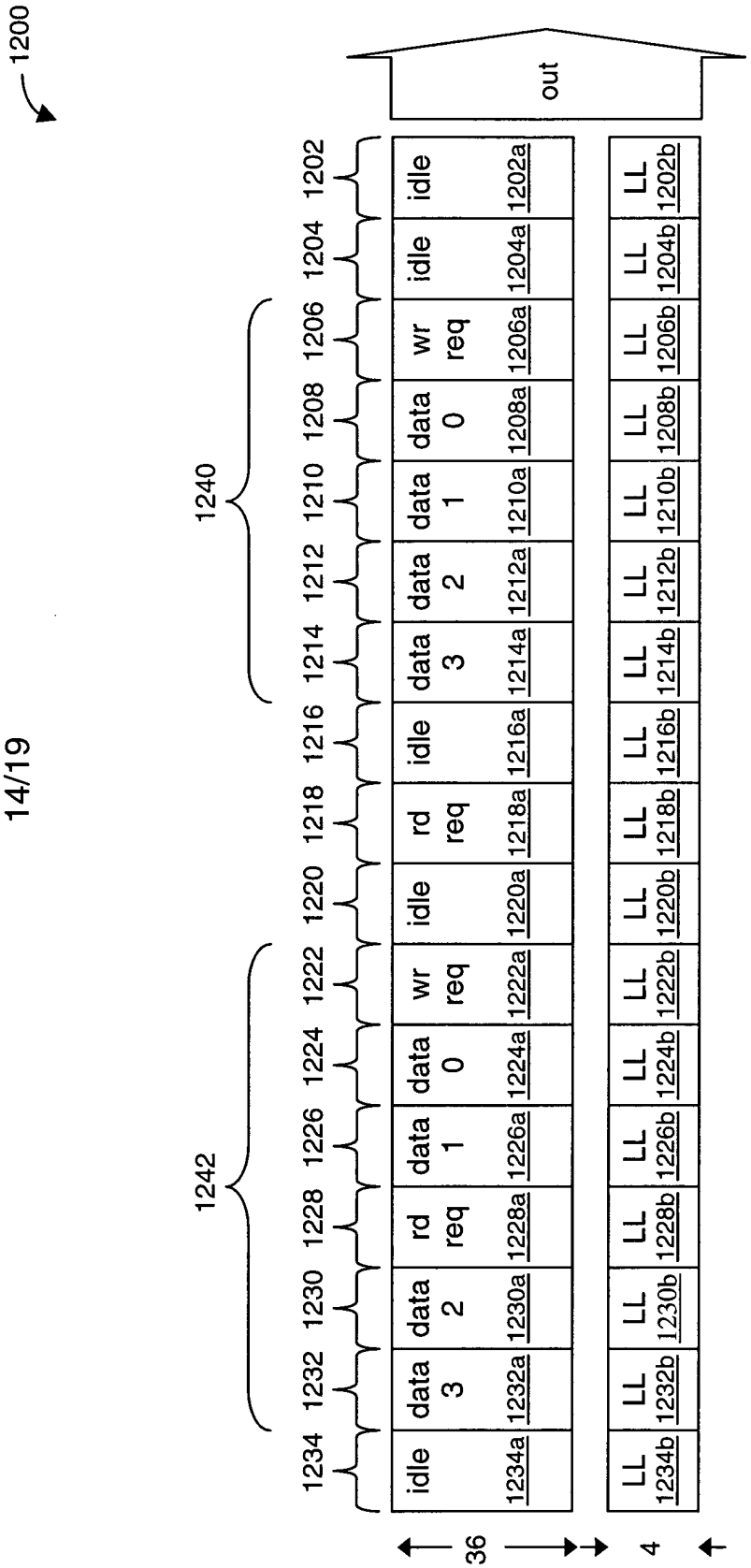
1200
out
1202
1204
1206
1208
1210
1212
1214
1216
1218
1220
1222
1224
1226
1228
1230
1232
1234
1240
1242
idle
data 3
data 2
rd req
data 1
data 0
wr req
idle
rd req
idle
data 3
data 2
data 1
data 0
wr req
idle
idle
1234a
1232a
1230a
1228a
1226a
1224a
1222a
1220a
1218a
1216a
1214a
1212a
1210a
1208a
1206a
1204a
1202a
LL
1234b
1232b
1230b
1228b
1226b
1224b
1222b
1220b
1218b
1216b
1214b
1212b
1210b
1208b
1206b
1204b
1202b
36
4

FIG. 12

1300

↓Transfer	BITS 17:0
0	Lower Order Address Bits and Read/Write Command
1	Higher Order Address Bits and Early Read Indicator
2	Command Destination, Offset from Address, Transaction ID, Check Bits, Mask Bits, Stream ID, Size Bits, Cancel Command, Priority, etc.
3	

FIG. 13

1400

↓Transfer	BITS 17:0
0	Lower Order Address Bits and Read/Write Command
1	Higher Order Address Bits and Early Read Indicator
2	Command Destination, Offset from Address, Transaction ID, Check Bits, Mask Bits, Size Bits, etc.
3	

FIG. 14

1500

↓Transfer	BITS 17:0
0	Lower Order Configuration Address Bits and Read/Write Command
1	Higher Order Configuration Address Bits and Early Read Indicator
2	Command Destination, Offset from Address, Transaction ID, Check Bits, Mask Bits, etc.
3	

FIG. 15

1600

LL signals	Transfers 0:3
0	Info and Check Bits
1	Header, Tail, and Check Bits
2	Extended Mode Bits
3	

FIG. 16

1700

LL signals	Transfers 0:3
0	Type and Check Bits
1	
2	Info and Check Bits
3	

FIG. 17

1800

LL signals	Transfers 0:3
0	Tag, Control, and Check Bits
1	
2	Tag, Info, and Check Bits
3	

FIG. 18

1900

LL signals	Transfers 0:3
0	Tag and Check Bits
1	
2	Tag, Info, and Check Bits
3	

FIG. 19

2000

LL signals	Transfers 0:3
0	Signal and Check Bits
1	
2	Signal, Info, Stop, and Check Bits
3	

FIG. 20